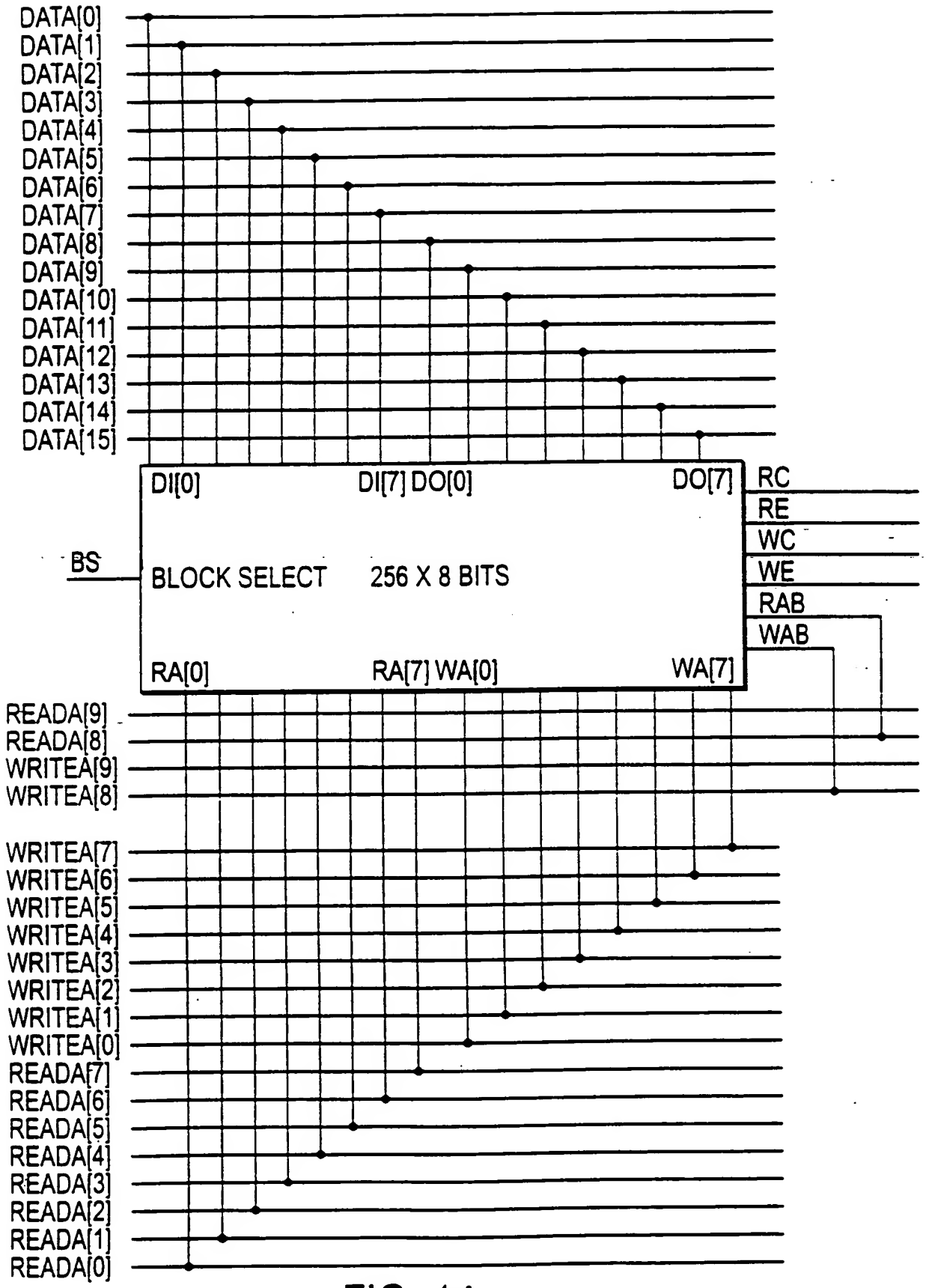


FIG. 1A (PRIOR ART)

FIG. 1B (PRIOR ART)

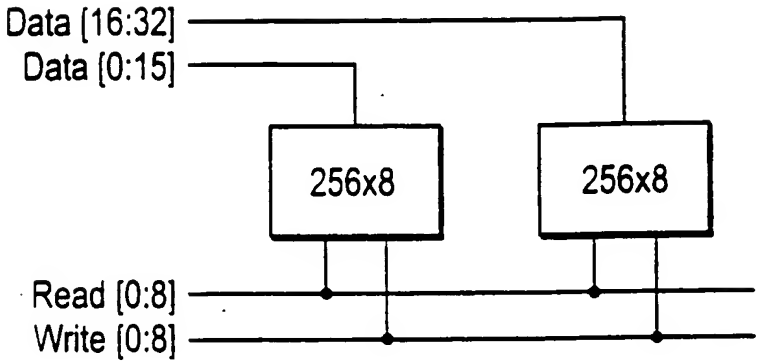
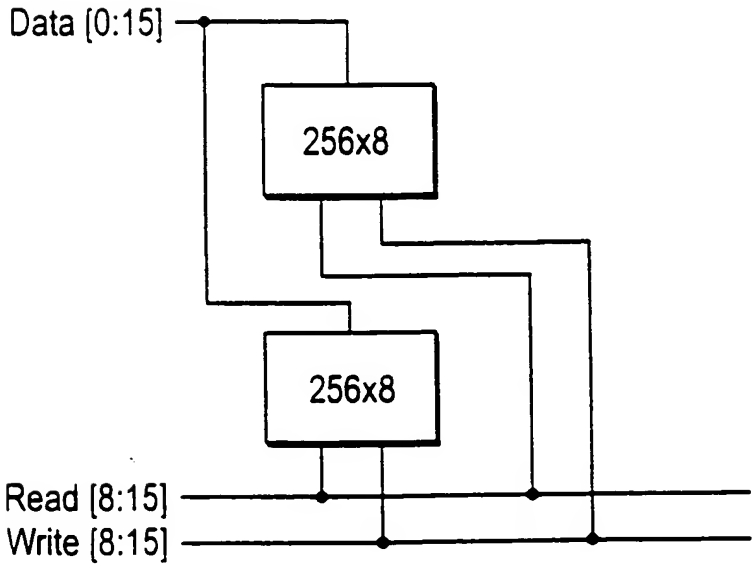


FIG. 1C (PRIOR ART)



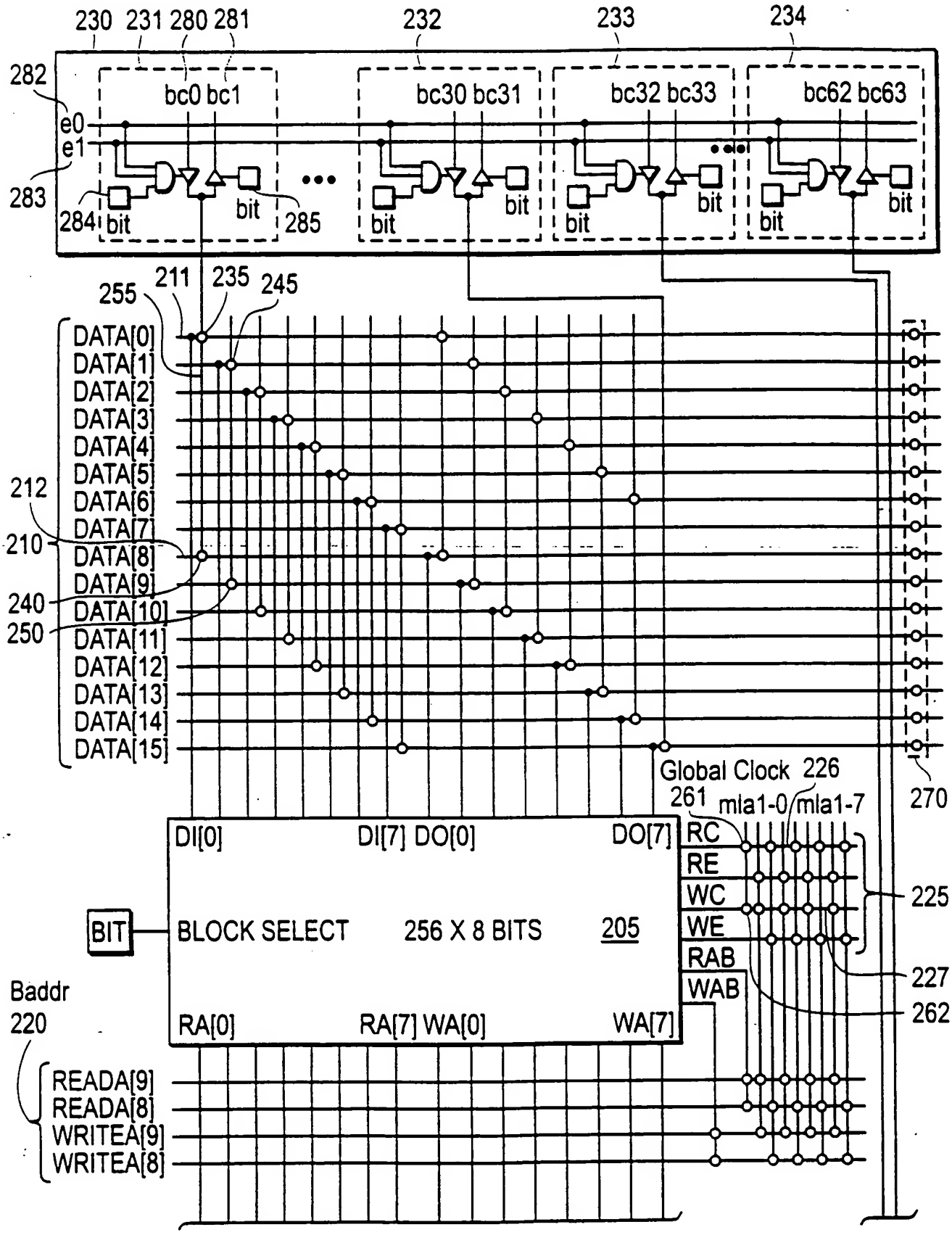

230
231
280
281
232
233
234
282
bc0 bc1
bc30 bc31
bc32 bc33
bc62 bc63
e0
e1
283
284
bit
285
255
211
235
245
DATA[0]
DATA[1]
DATA[2]
DATA[3]
DATA[4]
DATA[5]
DATA[6]
DATA[7]
DATA[8]
DATA[9]
DATA[10]
DATA[11]
DATA[12]
DATA[13]
DATA[14]
DATA[15]
212
210
240
250
Global Clock
226
261
mla1-0
mla1-7
270
DI[0]
DI[7]
DO[0]
DO[7]
RC
RE
WC
WE
RAB
WAB
225
227
262
BIT
BLOCK SELECT
256 X 8 BITS
205
Baddr
220
RA[0]
RA[7]
WA[0]
WA[7]
READA[9]
READA[8]
WRITEA[9]
WRITEA[8]

FIG. 2B ↓

FIG. 2A

FIG. 2A

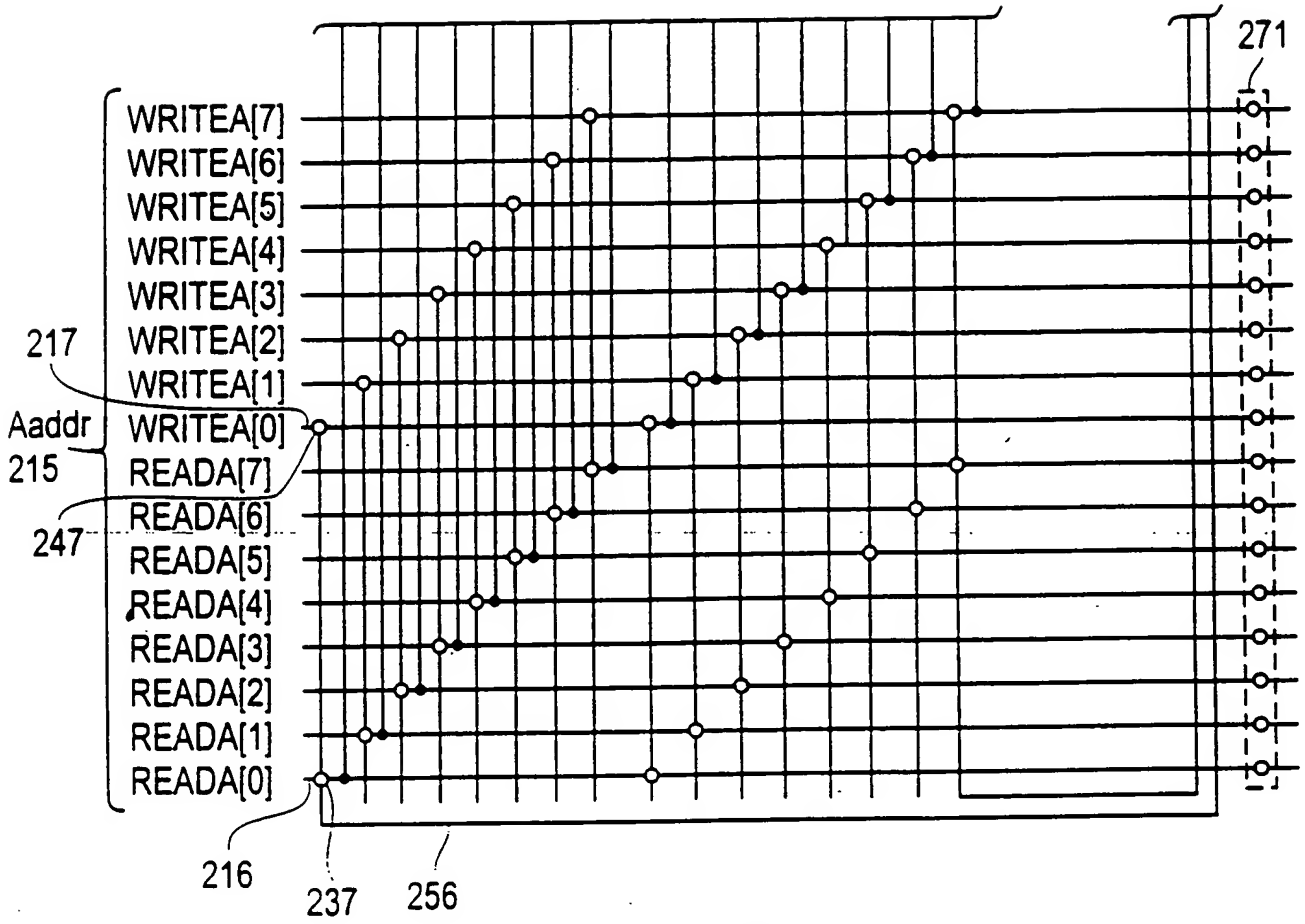

271
WRITEA[7]
WRITEA[6]
WRITEA[5]
WRITEA[4]
WRITEA[3]
WRITEA[2]
WRITEA[1]
WRITEA[0]
READA[7]
READA[6]
READA[5]
READA[4]
READA[3]
READA[2]
READA[1]
READA[0]
217
Aaddr
215
247
216
237
256

FIG. 2B

FIG. 3

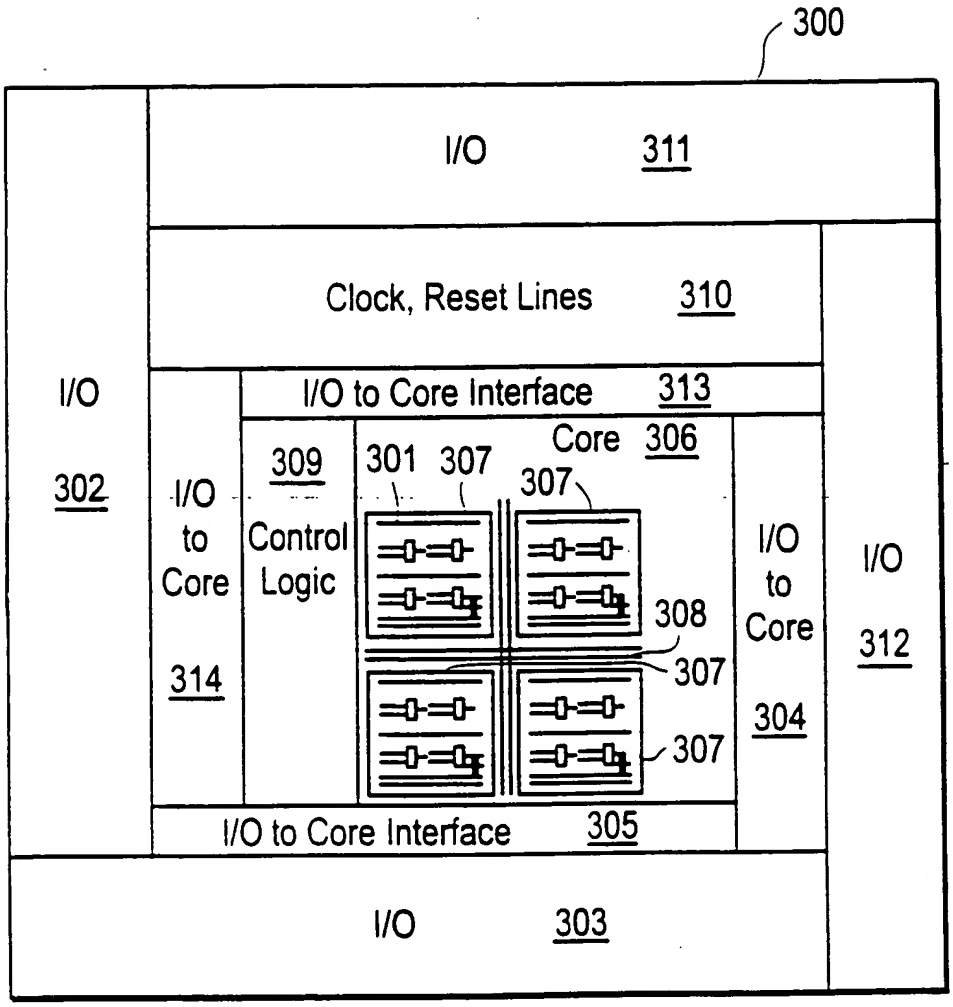

300
I/O 311
Clock, Reset Lines 310
I/O 302
I/O to Core Interface 313
309
Control Logic
301
307
Core 306
307
308
307
307
I/O to Core 314
I/O to Core 304
I/O 312
I/O to Core Interface 305
I/O 303

FIG. 4A

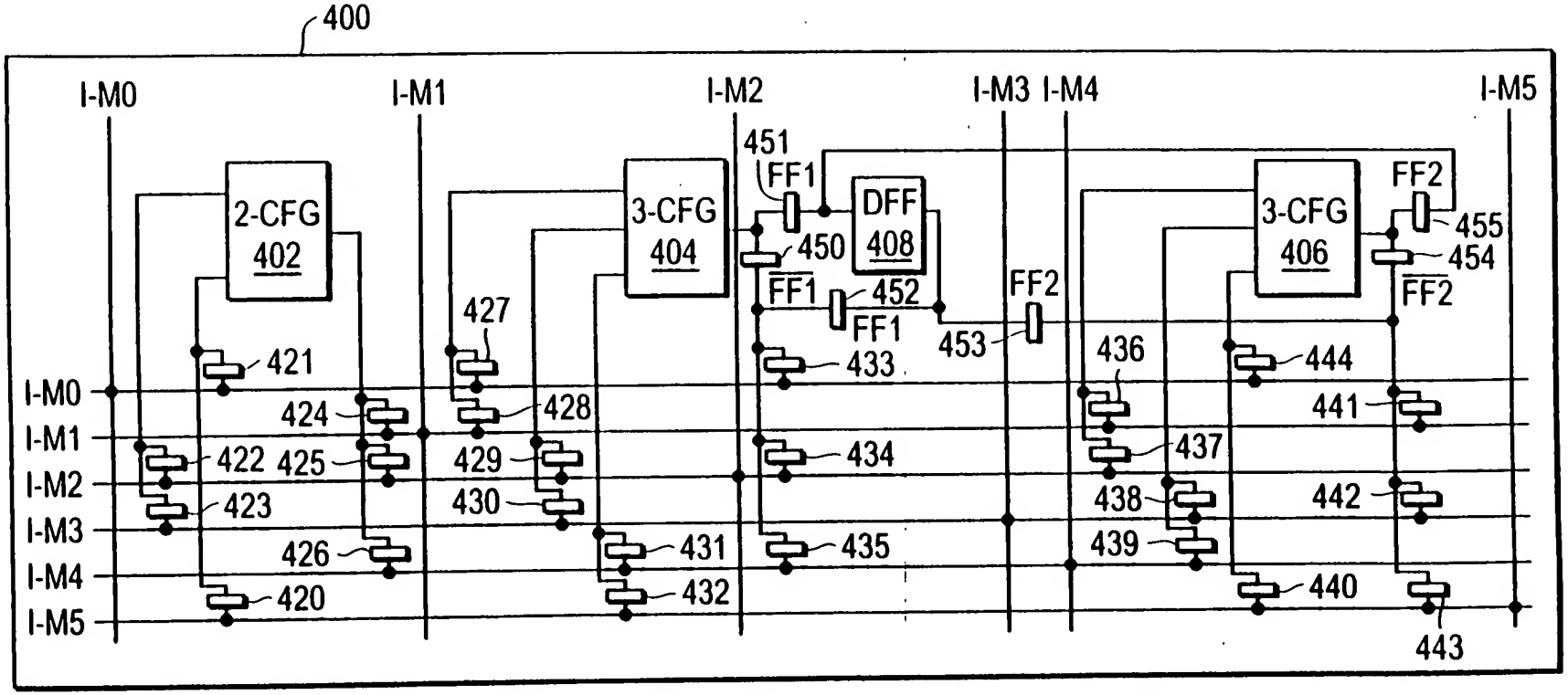

400
I-M0
I-M1
I-M2
I-M3
I-M4
I-M5
2-CFG
402
3-CFG
404
DFF
408
3-CFG
406
FF1
FF2
451
450
452
453
454
455
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444

FIG. 4B

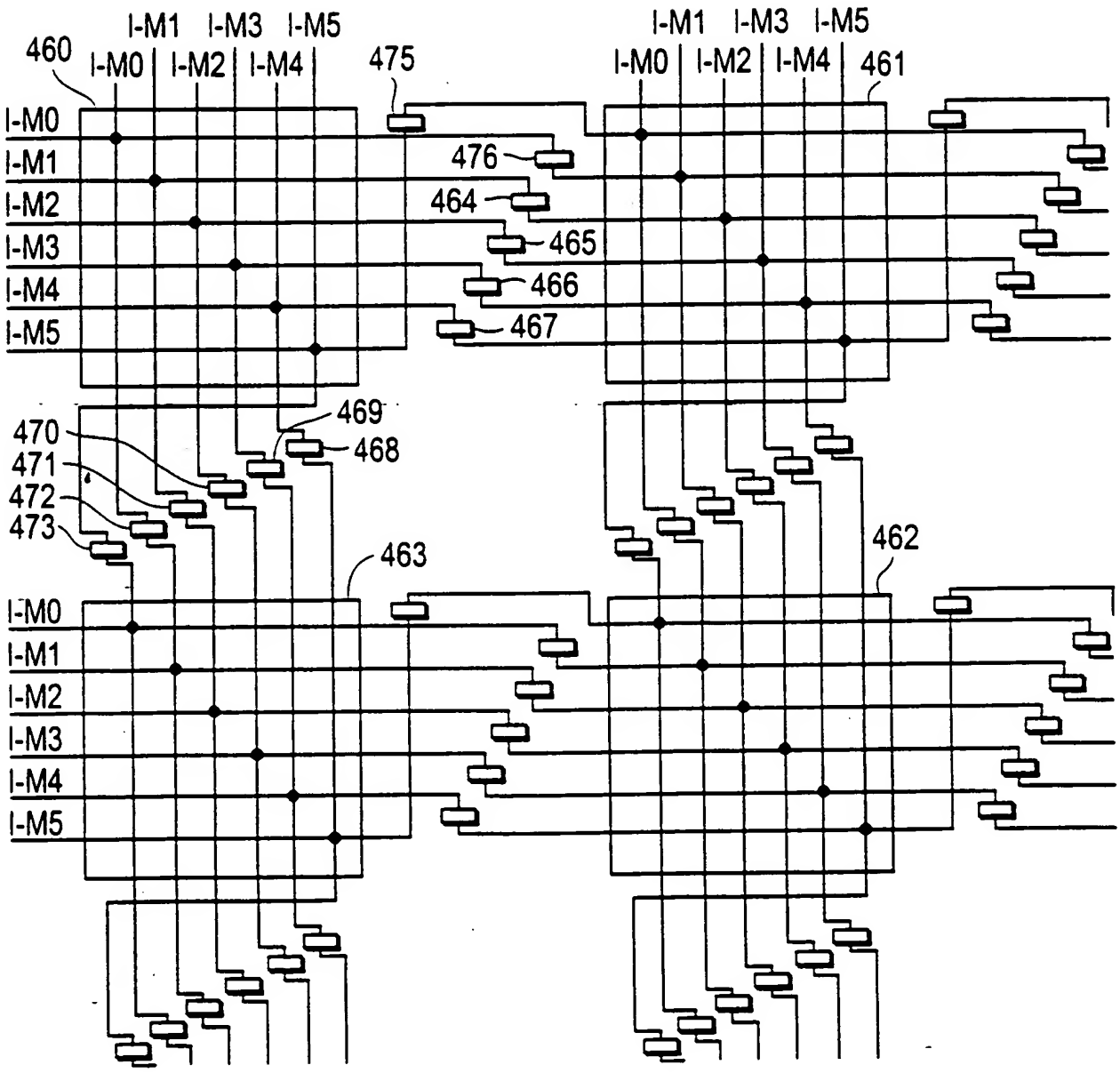

460
I-M0
I-M1
I-M2
I-M3
I-M4
I-M5
475
476
464
465
466
467
461
469
468
470
471
472
473
463
462

FIG. 5A

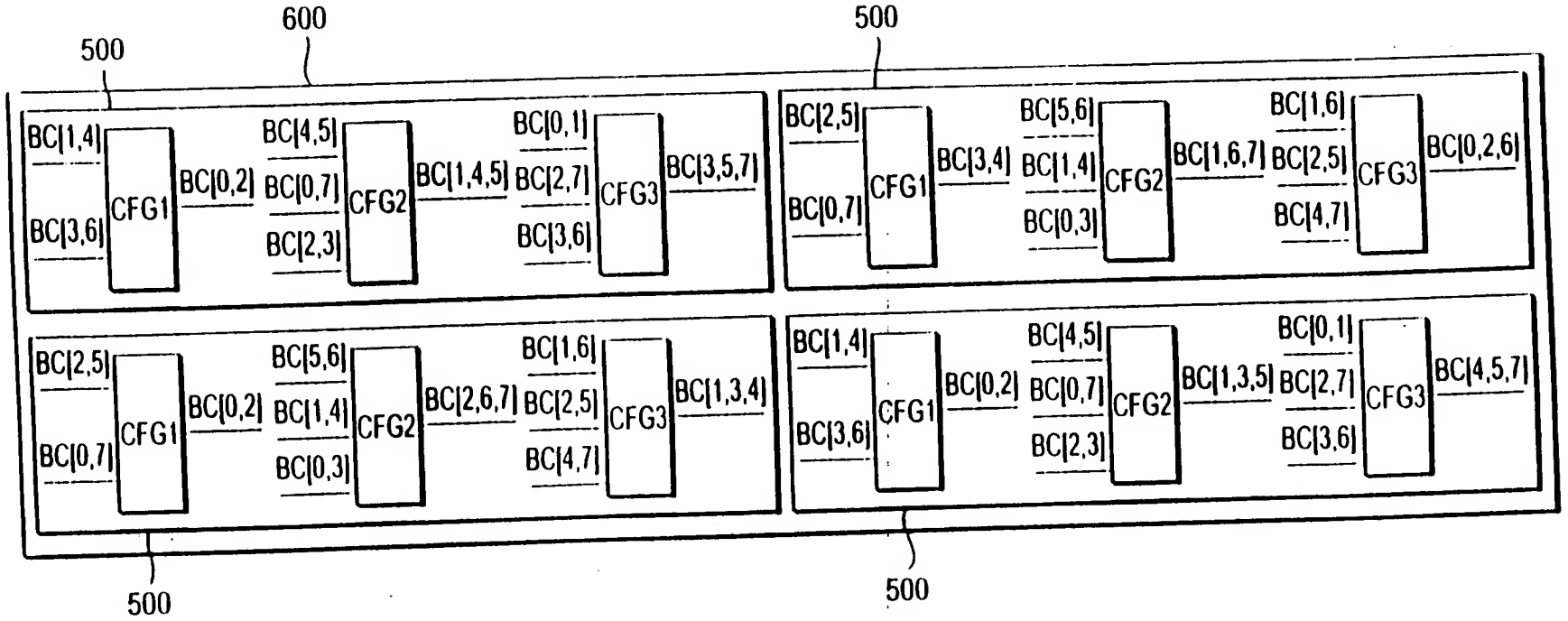

600
500
500
500
500
BC[1,4]
BC[3,6]
CFG1
BC[0,2]
BC[4,5]
BC[0,7]
BC[2,3]
CFG2
BC[1,4,5]
BC[0,1]
BC[2,7]
BC[3,6]
CFG3
BC[3,5,7]
BC[2,5]
BC[0,7]
CFG1
BC[3,4]
BC[5,6]
BC[1,4]
BC[0,3]
CFG2
BC[1,6,7]
BC[1,6]
BC[2,5]
BC[4,7]
CFG3
BC[0,2,6]
BC[2,5]
BC[0,7]
CFG1
BC[0,2]
BC[5,6]
BC[1,4]
BC[0,3]
CFG2
BC[2,6,7]
BC[1,6]
BC[2,5]
BC[4,7]
CFG3
BC[1,3,4]
BC[1,4]
BC[3,6]
CFG1
BC[0,2]
BC[4,5]
BC[0,7]
BC[2,3]
CFG2
BC[1,3,5]
BC[0,1]
BC[2,7]
BC[3,6]
CFG3
BC[4,5,7]

FIG. 5B

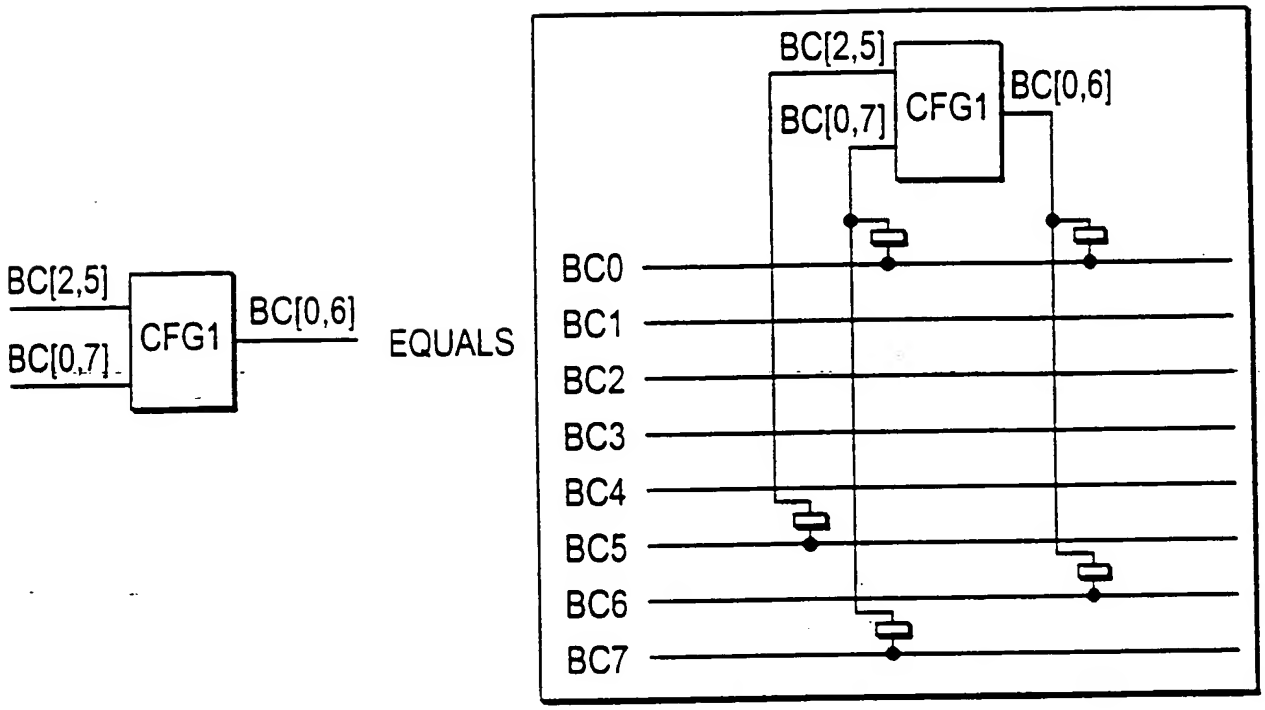

BC[2,5]
BC[0,7]
CFG1
BC[0,6]
EQUALS
BC[2,5]
BC[0,7]
CFG1
BC[0,6]
BC0
BC1
BC2
BC3
BC4
BC5
BC6
BC7

FIG. 6

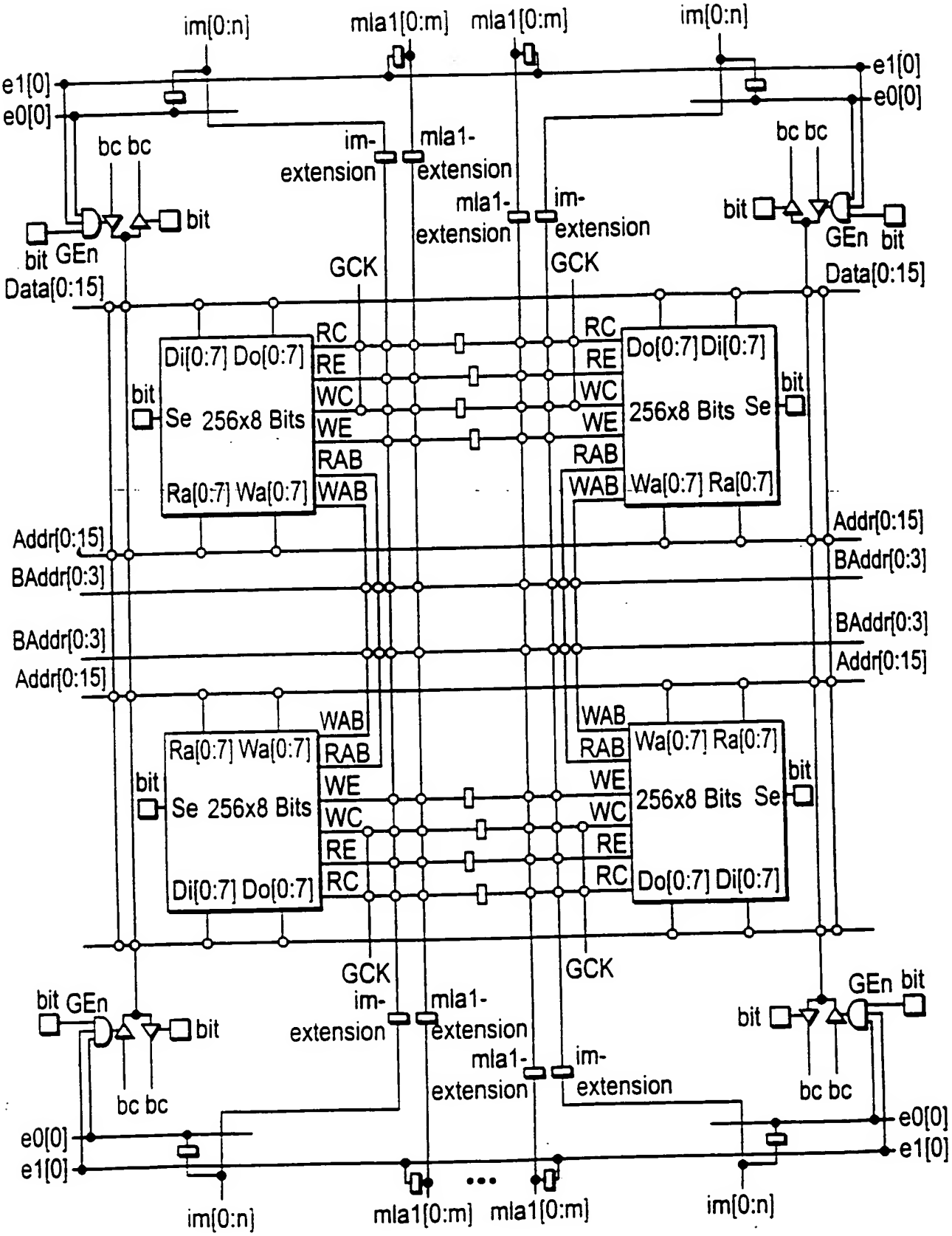

im[0:n]
mla1[0:m]
mla1[0:m]
im[0:n]
e1[0]
e0[0]
bc bc
im-extension
mla1-extension
mla1-extension
im-extension
bit
bit GEn
GCK
GCK
Data[0:15]
Di[0:7] Do[0:7]
Se 256x8 Bits
Ra[0:7] Wa[0:7]
RC
RE
WC
WE
RAB
WAB
Do[0:7] Di[0:7]
256x8 Bits Se
Wa[0:7] Ra[0:7]
Addr[0:15]
BAddr[0:3]
GEn bit
Ra[0:7] Wa[0:7]
Se 256x8 Bits
Di[0:7] Do[0:7]
Wa[0:7] Ra[0:7]
256x8 Bits Se
Do[0:7] Di[0:7]
im[0:n]
mla1[0:m]
mla1[0:m]
im[0:n]

FIG. 7B

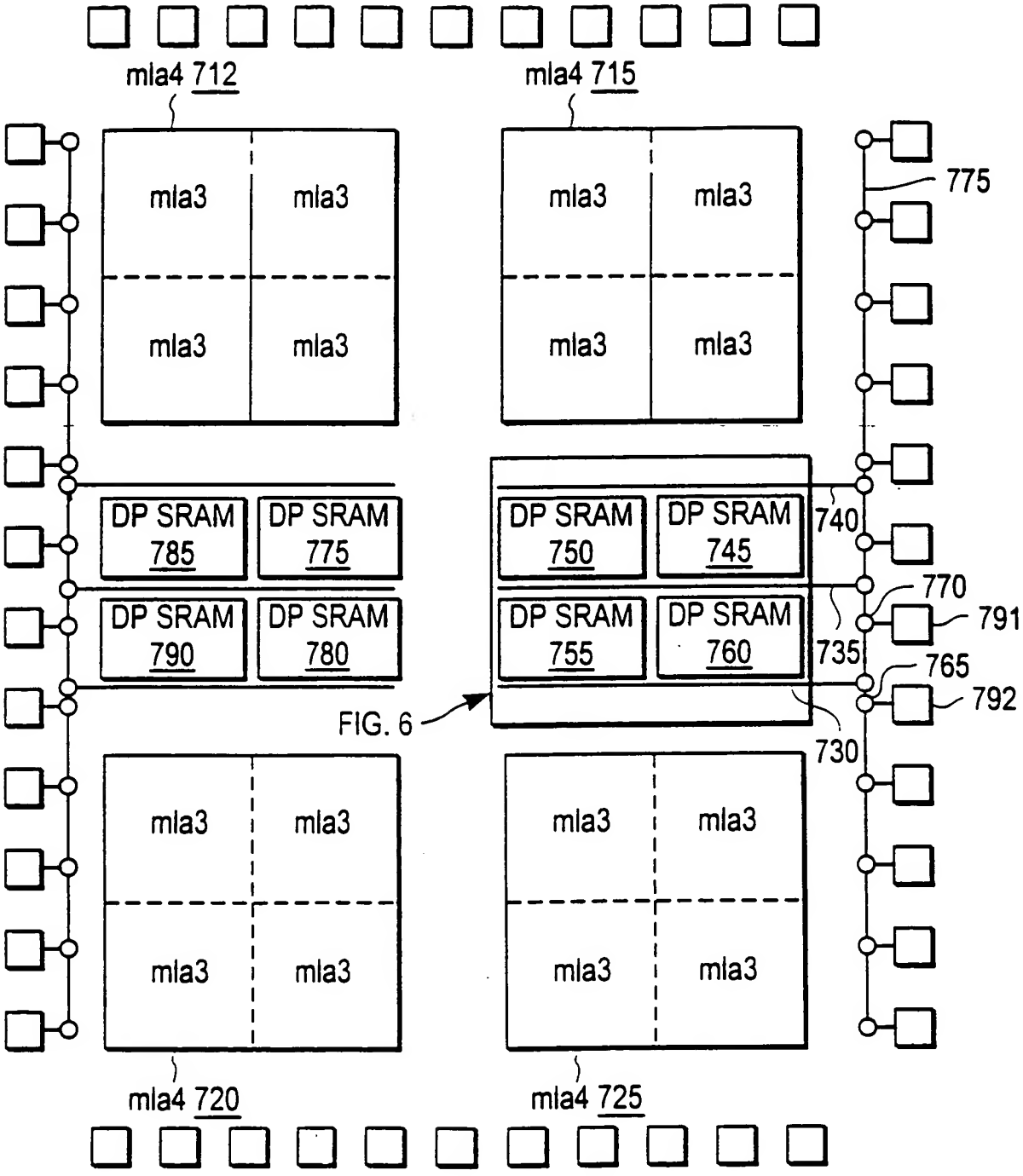
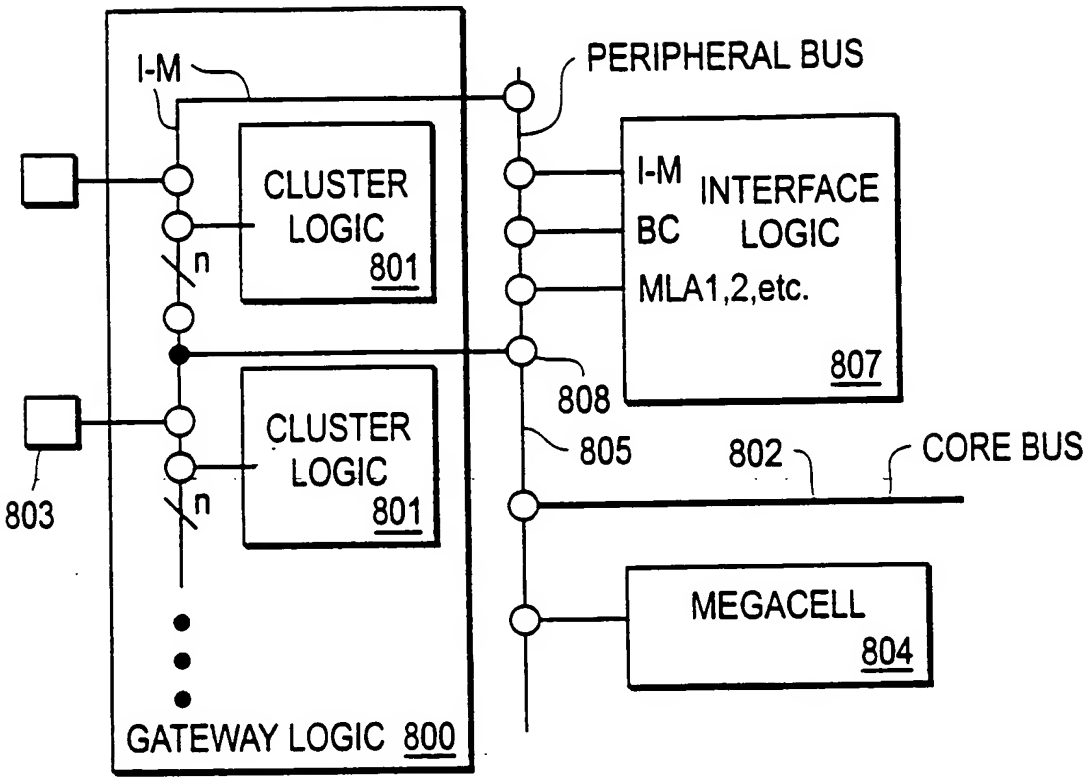

mla4 712
mla4 715
mla3
mla3
mla3
mla3
mla3
mla3
mla3
mla3
775
DP SRAM 785
DP SRAM 775
DP SRAM 790
DP SRAM 780
DP SRAM 750
DP SRAM 745
DP SRAM 755
DP SRAM 760
740
770
791
735
765
792
730
FIG. 6
mla3
mla3
mla3
mla3
mla3
mla3
mla3
mla3
mla4 720
mla4 725

FIG. 8A



○ : Each can be bi-directional, tri-statable

FIG. 8B

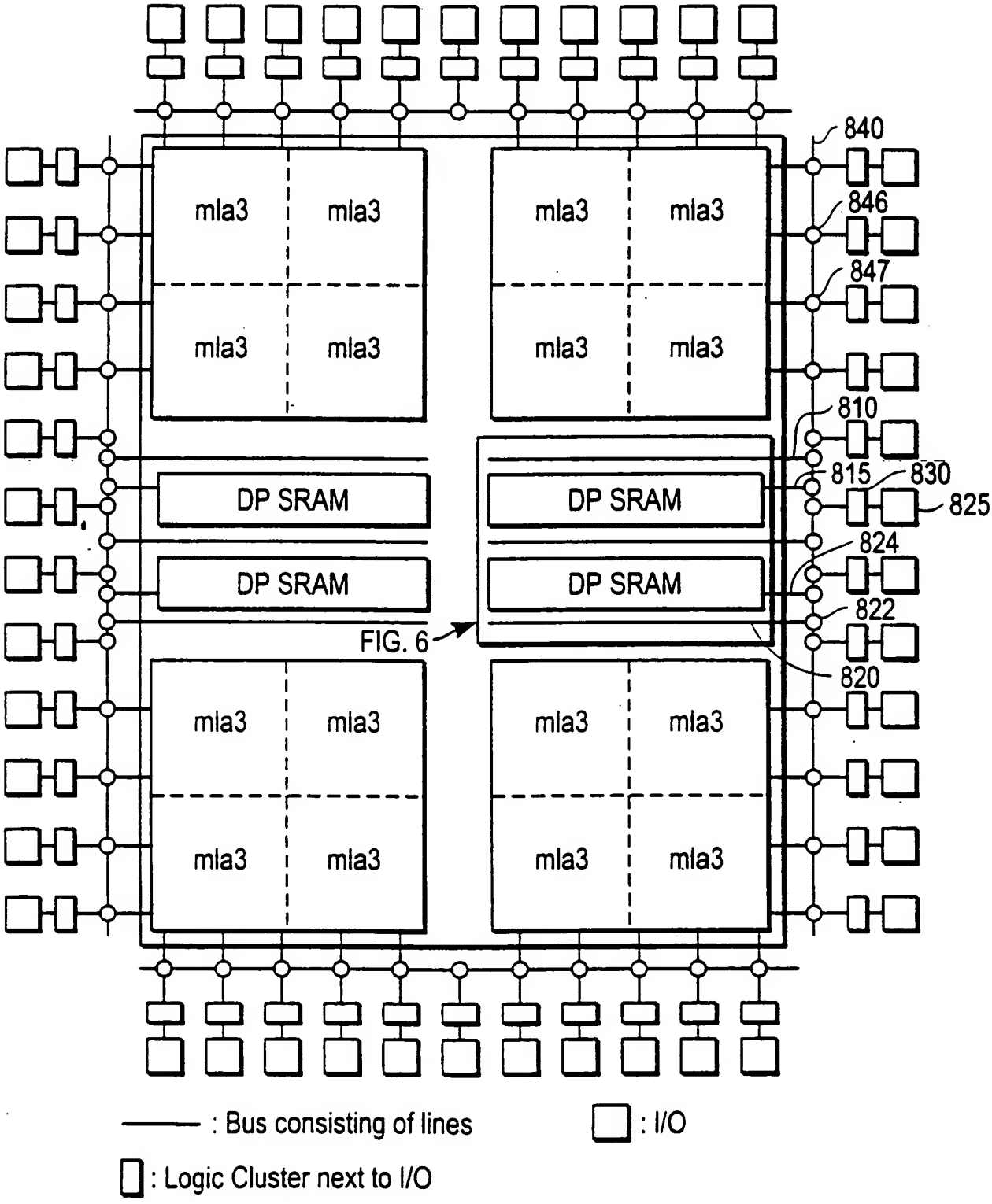
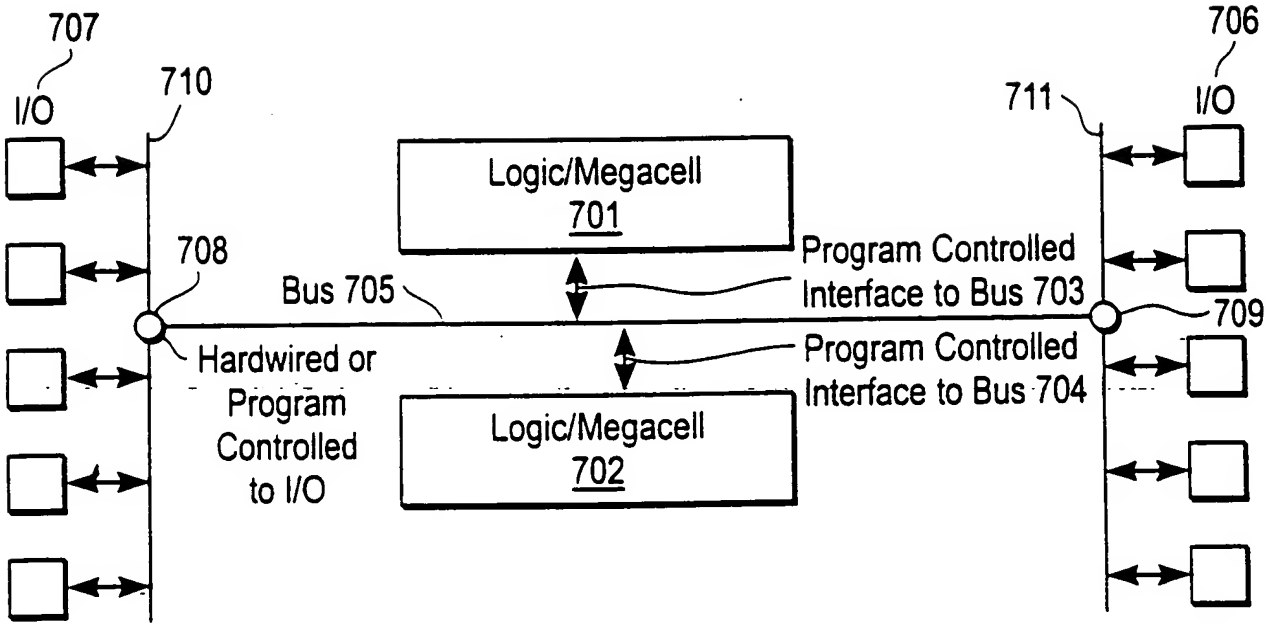

mla3
DP SRAM
FIG. 6
840
846
847
810
815
830
825
824
822
820
: Bus consisting of lines
: I/O
: Logic Cluster next to I/O

FIG. 7A


707
I/O
710
708
706
I/O
711
709
Logic/Megacell
701
Bus 705
Program Controlled
Interface to Bus 703
Hardwired or
Program
Controlled
to I/O
Program Controlled
Interface to Bus 704
Logic/Megacell
702